

^^ NOTE THAT THE COLUMN ORDER IS REVERSED FROM THE WAY IT IS ON THE HW

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 07/20/2022 12:31:09 PM

// Design Name:

// Module Name: QCounter

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module QCounter #(parameter word\_size = 4)

(output reg [word\_size -1: 0] CNT, input CLK, RST);

always @ (posedge CLK, posedge RST)

if (RST) CNT <= 0;

else CNT <= {CNT[word\_size-2:0],~CNT[word\_size-1]};

endmodule

//===============TESTBENCH ====================

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 07/20/2022 12:42:28 PM

// Design Name:

// Module Name: QCounter\_tb

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module QCounter\_tb(

);

reg CLK, RST;

wire [3:0] CNT;

QCounter UUT(

.CNT(CNT),

.CLK(CLK),

.RST(RST)

);

initial

begin

CLK=0;

RST=0;

forever #5 CLK=~CLK;

end

initial

begin

RST=1;

#1

RST=0;

#100

$finish();

end

endmodule